IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Inventor	:	G. Ramanath, et al.	Art Unit.	:	2813
Serial Number	:	10/809,317	Examiner	:	RODGERS, Colleen E.
Filed	:	03/24/2004		:	
Title	:	DIFFUSION BARRIERS COMRPISING SELF-ASSEMBLED MONOLAYERS		:	
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CERTIFICATE OF MAILING or FACSIMILE TRANSMISSION UNDER 37 C.F.R. § 1.8(a)(1)
I hereby certify that this correspondence (along with any referred to as being attached or enclosed) is, on the date shown below, being deposited with the United States Postal Service with sufficient postage as first class mail in an envelope addressed to Mail Stop Amendment, Commissioner for Patents, P.O. Box 1450, Alexandria Virginia, 22313-1450, or facsimile transmitted to the U.S. Patent and Trademark Office on the date shown below.

Dated: 9/11/06 By: Will Dresser

Printed Name: Will Dresser

DECLARATION OF RAMANATH GANAPATHIRAMAN UNDER 37 C.F.R. 1.132

Mail Stop RCE
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

I, Ganapathiraman Ramanath, Associate Professor of Materials Science & Engineering, Rensselaer Polytechnic Institute, 110 8th Street, Troy, NY 12180, USA, declare as follows:

1. I am a co-inventor of the subject patent application. My CV is attached hereto as Exhibit A.

2. I have reviewed the present application and the amendment accompanying this declaration.

3. As described in the present application, the presently claimed methods involve the formation of devices wherein copper is used as a conductive metal in an integrated circuit having an underlying substrate of a silicon material. It is an art recognized problem that such devices suffer from failure due to migration of copper atoms into the silicon. The present methods use a diffusion barrier that has been tested and found to prevent such failure.

4. Fig. 2 of the application shows the results of testing subunit 5 and subunit 10, showing much superior times to failure under conditions accepted in the art as simulating this failure, namely bias temperature testing at 2MV/cm and 200 deg. C. The time to failure of subunits 5 and 10 (having a pyridine and a benzyl ring, respectively) was found to be unexpectedly and significantly greater than either the control or subunits 8 and 9 (having no R2 and an alkyl head group, respectively.

5. Calvert et al. US 5,389,496 does not disclose a diffusion barrier. It discloses a bonding layer for bonding a catalyst to a substrate. The bonding layer may be formed by coating with β-trimethoxysilylethyl-2-pyridine, or other materials. The patent does not state that this material forms a self-assembled monolayer. The patent does state that the pyridyl group has been found to be a preferred ligating group for a palladium catalyst (a catalyst being necessary for electroless plating). One would not be motivated to use copper as a catalyst in this method.

6. Although the patent states that "it is believed that a wide variety of metals may be electrolessly plated in accordance with the present invention," Calvert et al. do not specifically disclose the use of a copper conductive layer, in that the only metal layers exemplified are nickel and cobalt.

7. The methods and materials disclosed in Calvert et al. would not result in a diffusion barrier, even if copper was electrolessly plated onto a silicon substrate according to the methods taught, for the following reasons:

(a) Immersion in a catalyst bath followed by a metallization bath would alter the properties of the adhesive molecular layer by modifying its terminal group--.i.e., the main vehicle that provides barrier properties.

(b) The copper layer resulting from electroless deposition has a poor morphology and poor adhesion, and different migration properties than those resulting from vapor deposition.

8. It would not be obvious to substitute vapor deposition for electroless plating in the methods taught by Calvert et al. The major reason for this is that the entire point of Calvert is to provide an improvement in electroless plating. There is no reason to carry out any f the steps of Calvert if one were using vapor deposition of copper on a silicon substrate, except for the reasons taught in the present application. Also introducing an additional metal layer, needed in Calvert/Schnur patents, is undesirable for several applications.

9. Electroless plating and sputtering are two completely different methods. **Electroless plating is not an obvious alternative method to vapor deposition**. For electroless plating, a catalyst layer on the substrate surface is typically needed to initiate metal deposition. However, no analogous procedure exists in a vapor deposition process (e.g., sputtering). Furthermore, in the electroless plating methods as disclosed in the references, the catalyst layer is seeded by a chemical reaction with a molecular layer found on the substrate in order to enable electroless metallization. It is well known that electroless metallization has a poor morphology and adhesion properties when formed on a molecular layer. **Any diffusion barrier properties of the molecular layer are likely to be neutralized by chemical reactions on the surface, such as reactions used in the process of forming the catalyst on the surface.**

10. The method by which the metal layer is deposited in the present invention is critical insofar as electroless plating will not work without damaging the barrier properties of the present self-assembled monolayer.

11. Schnur et al. US 5,079,600 also uses electroless plating. Schnur et al. teach the use of a self-assembling film that is chemically absorbed on the substrate's surface. The chemical reactivity in regions of the ultra-thin film is altered to produce a desired pattern in the film. A catalytic precursor, which adheres only to those regions of the film having enough reactivity to bind the catalyst, is applied to the film's surface. The catalyst coated structure is then immersed in an electroless plating bath where metal plates onto the regions activated by the catalyst.

12. Schnur et al. in Example 24, disclose the use of UTF3 (4--minobutyldimethylmethoxysilane). The film was patterned using a mask with standard capacitor test structures and irradiated for 28 minutes with an Hg/Ar lamp. The wafer was metallized with electroless plating. "The metal/thermal oxide/n-type silicon (MOS) capacitors were then characterized by probing the metal pads and the back of the wafer with a Micromanipulator automatic C-V measuring system. The capacitance was found to be 26 pF/cm^2 with minimal (10 mV) hysteresis and remained stable at room temperature for at over 3 weeks, indicating that device degradation due to masked metal contamination (diffusion of copper into the thermal oxide) was not a problem."

13. It has been shown since that C-V hysteresis alone (in the absence of other corroborating measurements such as leakage current, Triangular voltage sweep spectroscopy-TVS etc.) is insufficient to claim lack of Cu contamination (e.g., see pages 347 and 348 of H. Kizil, G. Kim, Ch. Steinbruchel, B. Zhao, C. Steinbruchel, J. Electron. Mat. **30**, 345-348 (2001). The room temperature test disclosed in Schnur et al. is not an adequate measure of diffusion barrier properties. Significant copper diffusion without electric fields occurs only above 100°C (for extended times) or 500-600°C for shorter times –in both cases without electric fields.

14. The devices produced by the methods of Schnur et al. are not inherently equivalent to the present devices because of the presence of an intervening catalyst layer between the Cu and the monolayer. Moreover, electroless Cu on Pd-ligated monolayer is chemically and physically distinct from Cu in direct contact with the monolayer.

15. I further declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code and that such willful false statements may jeopardize the validity of the application or any patent issuing thereon.

Signature /Ramanath Ganapathiraman/

Ganapathiraman Ramanath

Signed at Troy, New York

September 11, 2006

G. RAMANATH

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EDUCATION

Ph.D. (1997)	Materials Science and Engineering, University of Illinois, Urbana, IL.
M.S. (1993)	Materials Science and Engineering, University of Cincinnati, OH.
B.Tech. (1990)	Metallurgical Engineering IIT, Madras (now Chennai), India.

APPOINTMENTS

5/03 –	Tenured Associate Professor, MS&E Department, RPI, Troy, NY
9/03 –	Associate Editor, IEEE Transactions on Nanotechnology
2/05 –	Editorial Advisory Board Member, Journal of Experimental Nanoscience
6/06 – 8/06	Visiting Professor, Indian Institute of Science, Bangalore, India
9/04 – 8/05	Visiting Professor, Max Planck Inst. for Solid State Research, Germany
7/04 – 9/04	Visiting Professor, International Center for Young Scientists, NIMS, Japan
7/98 – 5/03	Tenure-track Assistant Professor, MS&E Department, RPI, Troy, NY
3/98 – 7/98	Visiting Scientist, Physics Department, Linköping University, Sweden
1/97 – 3/98	Member of Technical Staff, Novellus Systems Inc, San Jose, CA

HONORS AND AWARDS

- Alexander von Humboldt Fellowship (2004).
- Prof. Bergmann Memorial Young Scientist Award, US-Israel Binational Science Foundation (2003).
- School of Engineering Research Excellence Award, Rensselaer Polytechnic Institute (2003).
- Early CAREER Award, National Science Foundation (2000).
- IBM Research Partnership Award–University Partnership Program—co-recipient (1999-2005).
- Recent works were highlighted in Small (12/04), Materials Today (1/05), Science News, Bus. Rev., Wash. Times, C&E News, local TV (Apr/May '02).
- MRS Graduate Student Award, MRS Fall Meeting, Boston, MA (December 1996).
- Ph.D. work was Technology News in Solid State Technology (2/97) & Wafer News (12/96).
- Best Poster, High-temperature Intermetallics Symposium, MRS Fall, Boston (Dec. 1992).

ADVISEE AWARDS (selected recent)

- MRS Graduate Student Gold Award (M.S. Raghuveer), Spring meeting, San Francisco, CA (Apr. 05)
- 1st prizes in graduate student (M.S. Raghuveer) and professional (Dr. A. Yan) categories, and micrograph contest (S. Agrawal), ASM-TMS Hudson-Mohawk Chapter (Nov. 2005).
- 1st prize, poster competition (M.S. Raghuveer, Dr. P. Victor), NY-Nanotech (Oct. 2004).
- Nominee, best poster—in top 6 out of 250— (Dr. Gopal Ganesan), MRS Spring, San Francisco (2003)

FIVE RELEVANT PUBLICATIONS (total ~100+, 1 book chapter, 7+ disclosures, 1 patent)

1. *Low-temperature templateless synthesis of single-crystal bismuth telluride nanorods*, A. Purkayastha, F. Lupo, S. Kim, T. Borca-Tasciuc, **G. Ramanath**, Adv. Mater. **18,** 496-500 (2006).
2. *Site-selective functionalization of carbon nanotubes*, M.S. Raghuveer (MRS Graduate Student Gold Medalist), A. Kumar, M. Frederick, G. Louie (high-school biology teacher), P. Ganesan, **G. Ramanath**, Adv. Mater. (2006) *in press* (has appeared online).
3. *Microwave-assisted single-step functionalization and derivatization of carbon nanotubes with nanocrystalline gold*, M.S. Raghuveer, S. Agrawal, Nikki Bishop (sophomore), **G. Ramanath**, Chem. Mater. (2006) *in press*.
4. *Directed growth and electrical-transport properties of carbon nanotube architectures on indium tin oxide films on silicon based substrates*, S. Agrawal, M. J. Frederick, F. Lupo, P. Victor, O. Nalamasu, **G. Ramanath**, Adv. Func. Mater. **15**, 1922-1926 (2005).

5. *Enhanced chemical ordering and coercivity in FePt alloy nanoparticles by Sb-doping*, Q. Yan, T. Kim, A. Purkayastha, P. G. Ganesan, M. Shima, **G. Ramanath**, Adv. Mater. **17**, 2233 (2005).

FIVE OTHER PUBLICATIONS

6. *Hybrid microstructures from aligned carbon nanotubes and silica particles*, S. Agrawal, A. Kumar, M. J. Frederick, **G. Ramanath**, Small **1**(8-9), 823-826 (2005). Coverpage feature
7. *Nanomachining carbon nanotubes with ion beams*, M. Raghuveer, P. Ganesan, M. Marshall, J. D'Arcy-Gall, I. Petrov, **G. Ramanath**, Appl. Phys. Lett. **84**, 4484 (2004).
8. *Irradiation induced magnetism in carbon nanostructures*, S. Talapatra, P.G. Ganesan, T. Kim, R. Vajtai, M. Huang, M. Shima, **G. Ramanath**, D. Srivastava, S.C. Deevi, P.M. Ajayan, Phys. Rev. Lett. 95, 097201-0 (2005).
9. *Organized assembly of carbon nanotubes*, B. Q. Wei, R. Vajtai, Y. Jung, J. Ward, Y. Zhang, **G. Ramanath,** P. M. Ajayan, Nature **416**, 495 (2002).
10. *Polyelectrolyte nanolayers as diffusion barriers for Cu metallization*, P.G. Ganesan, J. Gamba (sophomore), A. Ellis, R. Kane, **G. Ramanath**, Appl. Phys. Lett. **83**, 3302 (2003).

GRADUATE STUDENTS AND POST-DOCTORAL ASSOCIATES

Current PhD students (5): M.S. Raghuveer, D. Gandhi, S. Agrawal, A.P. Singh, B. Singh
Graduated (8): H. Kim (PhD, 2005), M. Frederick (PhD, 2003), M. Stukowski (MS, 2003), G. Cui (MS, 2002), X. Guo (MS, 2002), X. Wang (MS, 2002), K. Chanda (MS, 2001), H. Goindi (MS, 2001)
Postdocs (3):, Dr. A. Yan, Dr. A. Purkayastha (co-advised), Dr. H. Li
Previous postdocs (12): Dr. A. Kumar, Dr. P. Victor, Dr. P.G. Ganesan, Dr. M. Frederick, Dr. Julie D'Arcy-Gall, Dr. Amanda Ellis, Dr. A. Cao, Dr. K. Vijayamohanan, Dr. R. Goswami, Dr. B. Wei, Dr. A. Krishnamoorthy, Dr. Z. Zhang.

UNDERGRADUATE STUDENTS Rensselaer URP, NSF-REU (**Total 28**)

A. Plate (RPI '06), A. Levin (RPI '06), N. Bishop (RPI '05), A. Wise(RPI '04), W. Joost (Spring, '03), S. Anderson (WSU., '03), L. Snedeker (Mich. Tech., '03), J. Reindieu (RPI, '03), J. Michalicek (RPI, '02), L. Underwood (RPI, '03), K. Dusling (Cooper Union, '02), Casey Rhodes (RIT), A. Giagnacova (Lincoln), O. Ahmadi (Yale), L. Klapp, (Cornell), T. Goeppinger, (U. Illinois), J. Patel ('03), C. Baid ('02), Erin McLellan ('01), J.-H. Kim ('01), J. Marzano ('01), R. Pang ('00), M. Ziegerhofer ('00) , D. Scholvin ('00), R. Leahy (Trinity Col., Ireland, '99), M. Wilkinson ('99), M. Stowe ('99), G. Verni ('99), J. Belfort ('98)

SYNERGISTIC ACTIVITIES

- *Associate editor*, IEEE Transactions on Nanotechnology (Oct 2003-)
- *Director*, NSF-REU summer program at MS&E Department (2001-2003)
- *Member*, US-Japan Young Scientist Exchange Visit Team in Nanotechnology (NSF-sponsored, 2003)
- *Symposium Chair*, "Nanofunctional materials", Nano 2006, Bangalore (2006); "Mesoscale architectures from nanounits: assembly, fabrication and properties", MRS Fall (2004); "Frontiers of thin films and coating technologies" International Conference for Metallurgical Coatings & Thin Films (2003-2006)
- *Conference Chair*, NY-NANOTECH (2002); *Board Member*, NY chapter of AVS (2002-2003)
- *Organized an 10-week internship* for a high-school biology teacher from New York City (2003). *Organized half-day long lecture demonstrations and site visits* for high-school and middle school students on exciting concepts in science, Knickerbacker High (2001), Shenendehowa Central (2000)
- *Created video-modules* on RBS and XPS for distance-learning graduate course (1999-2003)
- *Judge*, MRS Graduate Student Awards (2002), Colombus Foundation Invention Award (1999)

COLLABORATORS OUTSIDE RENSSELAER

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THESIS ADVISORS

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2. M.S.: Prof. V.K. Vasudevan, Dept. of Materials Science and Eng., University of Cincinnati, OH.